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FINAL REPORT

APPLICATIONS OF THIN FILM TRANSISTORS TO DIGITAL CORRELATION TECHNIQUES

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DEPARTMENT OF THE NAVY
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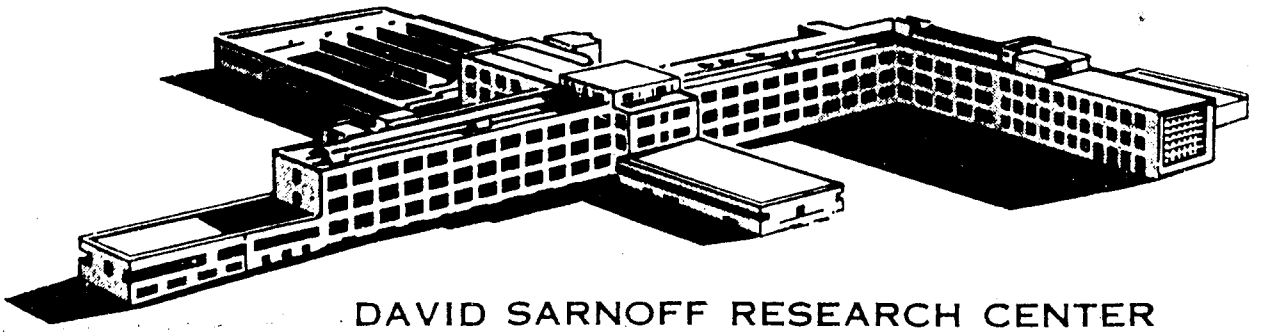

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ABSTRACT

The objective of this work was to demonstrate the suitability of thin film transistors (TFT's) to digital circuit applications, and to fabricate integrated arrays of TFT's during a later phase. A register of TFT flip-flops and comparator circuitry was chosen as a suitable test vehicle. Initial work was to be with individual TFT's while ultimately the entire register and comparator circuitry would be integrated.

Unexpected difficulties in producing large quantities of good TFT's delayed the evaluation of the operation of the register. The primary difficulty was the drift in the transconductance (g_m) of the units. Nevertheless a register was built and tested. The flip-flops used were capable of switching at 4 mc when overdriven from a low impedance source. A 1 mc rate was achieved when driven from a high impedance source. The internal speed of the TFT was determined to be in the nanosecond range, the operating speed being limited primarily by the input electrode and feedback capacitance.

Masks and jigs to fabricate the TFT in integrated circuits were prepared but fabrication of individual TFT's (in batches of 4-14) took precedence to facilitate the studies on the drift of characteristics.

It is currently possible to make batches of TFT's that have reproducible characteristics from batch to batch. The downward drift in the g_m remains a primary problem however, and is the subject of continuing research.

Concurrent to the development of the TFT, a new insulated gate transistor, the Metal-Oxide-Semiconductor (MOS) unit became available. This unit has characteristics similar to the TFT and can be used interchangeably with the TFT. Its characteristics are more stable than those of the TFT at present and it promises to be most useful in integrated circuits.

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I. INTRODUCTION

A method of fabricating transistors entirely by deposition of thin films upon an insulating support has long been desired, particularly because of the impact such a development would make upon the design of computers and integrated circuits. For the past two years a comprehensive research program with this objective has been carried on at RCA Laboratories originally supported in part by a government contract on high speed computers.[1]

The extremely short lifetime of minority carriers ordinarily found in thin evaporated layers of semiconductors suggested that the best prospect for producing transistors by evaporation lay in the control of majority carriers. A theoretical investigation[2] had indicated that with proper design a majority carrier device should have ultimate performance characteristics fully equal to that of a bipolar transistor. Furthermore, a unipolar transistor offers certain unique advantages for computers in the design of logic elements.[3]

The long background of work at RCA Laboratories on space-charge-limited currents in insulators,[4,5] led to the choice of cadmium sulfide as a most promising material for exploratory studies on active thin film devices. Previous workers had shown[6] that an "ohmic" contact to an insulating cadmium sulfide crystal can inject majority carriers (electrons) into the crystal thereby increasing its conductivity by orders of magnitude. An analogue-type transistor[7]

[1] Contract No. NObsr-77523

[2] Supplement to Interim Research Report 8A for High Speed Data Processor Systems Research, Contract No. NObsr-77523, December 1, 1960, pp. S-15 to S-31

[3] Wallmark and Marcus, IRE Transactions on EC, Vol EC-8, 98 (June 1959)

[4] A. Rose, Physical Review, 97, 1538 (1955)

[5] Rose and Lampert, Physical Review, 113, 1227 (1959)

[6] R. W. Smith and A. Rose, Physical Review, 97, 1531 (1955)

[7] W. Ruppel and R. Smith, RCA Review, 20, 702 (1959)

and a phototransistor[8] using cadmium sulfide crystals have been reported, but their performance was relatively poor owing to the low mobilities in cadmium sulfide. Fortunately, a background of experience at RCA Laboratories in the evaporation of thin films[9] and fine patterns[10] for television pickup tubes has contributed to the successful construction of evaporated transistors[11] in which the effect of low mobilities normally found in microcrystalline layers is compensated by the use of electrodes of extremely close spacing.

The results obtained have been of far-reaching significance. New techniques of evaporation have been developed which extend the frequency capabilities of the device and ease still further the requirements on the materials. At the same time, significant advances have been made in the processing of evaporated semiconductor layers to improve the electrical characteristics of the materials. Such devices have been made to oscillate at frequencies up to 17 megacycles. With further improvements in technology and materials, very large gain bandwidth products are expected. The relative fabrication simplicity of this evaporated thin film transistor (TFT) makes it an outstanding candidate for digital processors requiring large numbers of active devices, particularly in integrated networks. In addition to being used as the logical element in digital processing equipment, the TFT may ultimately be so inexpensive that it becomes economically feasible to use it in high speed content addressable memories.

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[8] R. Bockemuehl, Proceedings of the IRE, 48, 875 (1960)

[9] P. K. Weimer, RCA Review, 12, (1951)

[10] P. K. Weimer, et al, IRE Transactions on EL Devices, 147 (July 1960)

[11] P. K. Weimer, "Evaporated Thin Film Triodes," paper presented at the Solid State Devices Research Conference, Stamford, June 1961

II. THIN FILM TRANSISTOR CHARACTERISTICS AND CIRCUITS

The thin film transistor (TFT) is an evaporated three terminal device with a volt-ampere characteristic similar to that of a vacuum tube pentode. That is, it has a high input impedance (gate to source) and a high output impedance (drain to source). The symbol used for a TFT is shown in Fig. 1a. A typical source-drain volt-ampere characteristic of a TFT operating in the enhancement mode is shown in Fig. 1b. The drain current is plotted as a function of drain voltage (with the source grounded) for different values of positive gate voltage. As seen from the figure, the drain current remains small for increasing gate voltage up to several volts after which it begins to increase rapidly. This phenomenon gives rise to a device transfer characteristic (drain current as a function of gate voltage) that is well suited to digital logic circuitry. The transconductance of the unit shown at high gate voltage is about 3000 micro-mhos.

At the present time the switching speed of the TFT is limited by the input capacitance. The gate to source capacitance is 50 - 100 pf and the gate to drain capacitance about 20 pf. When the Miller effect is considered, a TFT with a transconductance of 2000 micro-mhos and a load resistance of 10 k ohms would have an effective gate to source or input capacitance of 500 pf. As a result of this large input capacitance a TFT amplifier driven from a 10 k ohm source (e.g. driving the amplifier by another TFT) has a time constant limited to a minimum of 5 microseconds. The gate to drain capacitance also causes a feedthrough of the leading and trailing edges of the input pulse to the output. The polarity of this feedthrough is opposite that of the TFT output and results in inverted spikes on the output pulse. Fig. 2 which shows the rise time of a TFT amplifier for several values of driving source impedance illustrates the effect of the input

capacitance. This large capacitance is due to the excessive overlap of the gate and source-drain electrodes. Improved masking techniques should make it possible to reduce this by an order of magnitude.

A. The TFT As A Logic Element

The high source-drain impedance when a TFT is off (low gate voltage) and low source-drain impedance when a TFT is on (high positive gate voltage) allow logic gates to be simply constructed with TFT's. Several TFT's in series with a common load resistor form a NAND gate as shown in Fig. 3a. The circuit output voltage is lowered only when all of the inputs are at a high positive value. The positive inputs cause the source-drain impedance of each TFT to become low, thus producing a reduction in circuit output voltage. As a result this circuit performs the logical AND-NOT function. Output waveforms of a two-input NAND gate are shown in Fig. 3b.

A NOR gate is formed by the series combination of a load resistor and several TFT's in parallel. A two input NOR gate is shown in Fig. 4a. The circuit output voltage is reduced to a low value when any one of the inputs is at a high positive value. The output waveforms of a two input NOR gate are shown in Fig. 4b. The fan-out of either type of logic gate is limited only by the input capacitance of the TFT's being driven. Thus large fan-outs can be obtained if the reduction in speed can be tolerated.

As discussed above, it is a simple matter to construct NAND and NOR logic gates. Since these two logic gates form a complete set, it is possible to construct any logic function with these gates. To determine how well these gates perform when operated in a combinational logic network, the circuit shown in Fig. 5a was constructed. This circuit consists of two two-input NAND gates each driving one input of a NOR gate. The NAND gates are in turn driven by

TFT amplifiers and the NOR gate drives a TFT amplifier. The output of this combinational network for several input combinations is shown in Fig. 5b. Each of the load resistors was optimized for best overall circuit performance.

B. The TFT As A Storage Element

The construction of flip-flops with TFT's as the active devices is simplified by the nature of the device. That is, no level shifting is necessary between the output of one TFT and the imput of the other. This is possible because a TFT amplifier output voltage and input voltage are both positive and have the same range of values. For example, an input of +2 volts produces an output of +8 volts and an input of +8 volts produces an output of +2 volts. As a result of this, two TFT's can be direct coupled to form a bistable flip-flop as shown in Fig. 6a. In order to provide a means of triggering the flip-flops, TFT's can be paralleled as shown in Fig. 6b. This method of triggering allows the input circuit to be in the form of an AND gate. That is, two inputs must be present to trigger the flip-flop. Such an input circuit could be used in a shift register where one input is the information from the previous stage and the other input is the shift pulse. As with other types of flip-flops it is also possible to use steering diodes for triggering. Flip-flops have been constructed using both types of triggering.

Fig. 7a shows the output waveforms of a flip-flop triggered by a TFT amplifier through steering diodes. The negative-going trigger is applied only to the gate of the TFT which is conducting. The maximum repetition rate of the flip-flops triggered in this manner was 100 kc. This frequency limit is caused by the reduced output voltage swing of the flip-flop. At this frequency the output voltage swing is such that the negative-going voltage is applied to the gate of the nonconducting TFT before the amplitude of the trigger voltage applied to the

conducting TFT is sufficient to cause the flip-flop to change state.

The maximum repetition rate of the set-reset flip-flop is not limited in this manner. When the flip-flop is operated in the set-reset mode, a pulse is applied to one side to set the circuit and then to the other side to reset the circuit. Several flip-flops have been operated in this manner. Waveforms of one such flip-flop triggered through diodes from two separate pulse generators are shown in Fig. 7b. Fig. 7c shows waveforms of the same circuit when the triggering is done with TFT's. That is, two TFT's are connected in parallel with the flip-flop TFT's - one on each side. The triggering pulses are then applied to the TFT gate terminals. The maximum frequency attainable with set-reset flip-flops was 4 mcs. This limit is set by the capacitance of the devices.

The transconductance of the TFT's used in the flip-flops ranged from 500 to 3000 micro-mhos. The circuit load resistance varried from 3 K to 15 K ohms. In order to match the TFT's so that a flip-flop could be constructed, the load resistors were made variable.

It is possible to determine statically from the TFT volt-ampere characteristic and the value of load resistance whether or not two TFT's can be made into a flip-flop. The procedure, given the value of load resistors and the supply voltage, is to draw the load line on the TFT volt-ampere characteristics and plot the resulting drain voltage as a function of gate voltage for one TFT and the gate voltage as a function of drain voltage for the other TFT. Since the TFT's are direct coupled in the flip-flop (the gate terminal of each TFT is directly coupled to the drain of the other TFT), the gate voltage of each TFT is the drain voltage of the other TFT. If the two curves are plotted on the same graph, the characteristic shown in Fig. 8a will be the result (assuming the TFT's will actually operate as a flip-flop). As seen in the figure, the two curves

intersect three times. The middle intersection is an unstable point corresponding to both TFT's conducting. The other two intersections correspond to the two stable states of the flip-flop. From this static flip-flop characteristic it is possible to determine the output voltage swing, necessary trigger amplitude, and noise immunity of the circuit. The effect of varying the value of the supply voltage and load resistances can also be obtained. Thus, it is possible to obtain the optimum value of load resistance for each TFT. The procedure used to obtain the flip-flop characteristic can be simplified by using an X - Y recorder and the circuit shown in Fig. 8b. This circuit allows any value of load resistance to be selected and the resulting curve plotted directly on the X - Y recorder.

A binary counter was constructed to test several flip-flops operating together. The counter was a scale-of-sixteen incorporating four TFT flip-flops. Each flip-flop was triggered through steering diodes from the output of the previous stage. The actual counter circuit is shown in Fig. 9. Due to the limited supply of TFT's it was only possible to operate the first two stages as a scale-of-four counter.

Although the supply of TFT's was limited, an end-around shift register complete with error detection was designed. A block diagram of the system is shown in Fig. 10. The write information is supplied to each stage of the shift register and the comparator circuits by means of toggle switches. The shifting of information from stage to stage is initiated by activating the clock pulse source. The clock pulses also operate a scale-of-n counter (n = the number of register stages). At the end of n shifts the counter produces an output which activates the comparator. The remaining input to the comparator is the information contained in the shift register. The comparator then determines, upon reception of the counter

output after the nth shift, if the present shift register information and the information from the input circuitry agree. If an error is present, the comparator produces an output which can be used to turn off the clock and/or provide a visual indication of an error.

One stage of the shift register and the means of error detection are shown in Fig. 11. The writing of information into the flip-flop is accomplished by supplying a positive voltage (logical "1") to one input of an AND gate. There are two such AND gates. Each one is in parallel with one of the flip-flop TFT's. A positive voltage, applied to the left AND gate will write in a "1" and the same voltage applied to the right gate will write in a "0". The write operation is completed by pulsing the remaining input to the AND gates with a write pulse. The application of the write pulse thus lowers the voltage on the left TFT for a "1" input or lowers the voltage on the right TFT for a "0" input. Writing in a "1" connects the left side of the flip-flop to the comparator AND gate. The writing in of a "0" connects the right side of the flip-flop to the comparator AND gate.

Shifting from left to right is done in a manner similar to the write operation. The previous stage output and its compliment are connected to each side of the flip-flop through two AND gates. The shifting is accomplished by pulsing the remaining input to the AND gates with the shift pulse, thus forcing the information of the previous stage into the flip-flop.

After n shifts, if the information contained in the flip-flop is the same as that written in before shifting, the input to the comparator AND gate will be low. If the information in the flip-flop is the compliment of the original information written into the stage, the input to the comparator AND gate will be high. Thus, the application of the counter pulse to the comparator AND gate after

n shifts will produce a comparator output if and only if the register stage does not contain the original information.

In anticipation of the shift register actually being constructed in integrated form, an evaporation layout of a stage of the shift register was made up. This layout is shown in Fig. 12. At the present time the techniques of TFT construction are not advanced enough to actually try to evaporate this circuit.

III. TFT ARRAY FABRICATION

A. Introduction

The TFT can be completely fabricated by successive vacuum depositions of conductors, semiconductors, and insulators. The fabrication steps and materials used are entirely compatible with those required in the fabrications of evaporated resistors, capacitors, and interconnecting wiring patterns. The introduction of a vacuum deposited active device thus makes technologically and economically feasible the construction of large integrated electronic circuits containing many active and passive elements on a single substrate. Some of the inherent problems associated with constructing integrated circuits of this type have been studied during the contract period in preparation for actual integrated digital circuit fabrication. A description of this investigation is presented below.

B. Review Of TFT Fabrications Steps

In order to appreciate the technological problems encountered in making integrated TFT circuits, it is helpful to review the basic steps taken in fabricating a TFT.

The TFT is a four-layered structure. In the most common form, source-drain electrodes separated by a narrow gap are deposited upon a flat, smooth insulating substrate. Cadmium sulfide, insulator, and gate electrode (in that order) are then deposited over the gap to complete the device. Fig. 13 shows the precision jig which holds the substrate during the electrode and insulator depositions. The jig has three essential parts: a) a substrate holder with provision for precise motion of the substrate; b) a wire grill frame; c) a moveable mask holder with provision for two masks. Figs. 14a, b, c, d show the four masks used in the fabrication of a TFT. Fig. 15 is a photograph of some TFT's made using these masks.

Fig. 16 shows the view from the substrate surface looking toward the evaporator during the source-drain deposition. The mask (Fig. 14a) determines the electrode configuration (the two small holes provide measurement terminals for the narrow gate electrode, which is deposited later). The single wire which divides the mask pattern is used to produce the required narrow gap in the following manner: The electrode metal is evaporated through the mask, past the wire onto the substrate, producing a gap between electrodes equal to the wire diameter. The substrate is then moved with respect to the wire a distance less than the wire diameter and more electrode metal is deposited. The resulting electrode gap has a dimension equal to the difference between the wire diameter and the distance moved.

The substrate, with source-drain electrode configuration, is then placed in a second vacuum system and cadmium sulfide is evaporated through a second mask (Fig. 14b). Finally, the substrate is placed again in the precision jig and insulator and gate electrode depositions are carried out through the masks shown in Figs. 14c and 14d respectively. (If an extremely narrow gate electrode is not required, the wire grill need not be present). Fig. 17 shows the turret evaporator used for all but the CdS evaporations.

It is worthwhile to note at this point that if a complete integrated circuit were the goal, the deposition of wiring and of capacitor and resistor electrodes could be accomplished simultaneously with either or both electrode depositions, the capacitor dielectric and insulating patches for wiring crossovers could be obtained during the insulator deposition, and cadmium sulfide resistive strips could be deposited during the cadmium sulfide evaporation. Thus no additional steps would be necessary to fabricate the complete circuit.

C. Problems Peculiar To Integrated Circuits

The cadmium sulfide TFT is a fait accompli. Simple integrated circuits such as single flip-flops or three-stage audio amplifiers have been built and tested with success.[12] Before integrated circuits containing large numbers of devices on a single substrate can be constructed and utilized in equipment, however, three things must be established.

1. Uniformity of device characteristics over a single substrate.
2. Reproducibility of device properties from substrate to substrate.
3. Feasibility of constructing large arrays of small precisely dimensioned and closely spaced devices on single substrates at reasonable cost.

The following is a discussion of the enbodiment of these problems in TFT fabrication.

1. Uniformity

The uniformity problems which arise have two origins: variation in the thickness and/or electrical properties of the CdS and pinholes in the insulating layer. The former arises chiefly because of temperature variation across the substrate.

2. Reproducibility

Dependable reproducibility of device properties from substrate to substrate requires the exact duplication of each step in the fabrication process. Factors such as evaporation rate, source and substrate temperatures, substrate cleanliness, source to substrate distance, vacuum conditions, evaporant purity, and thicknesses of evaporated layers all affect the device properties in varying degrees, and hence must all be controlled. In addition, since the present sequence of fabrication steps requires exposing the partially completed substrate to atmospheric conditions between evaporations, these atmospheric conditions

[12] P. K. Weimer, Proceedings of the IRE, 50, 1462 (1962)

(e.g., humidity) play a determining role.

3. Device Dimensions and Precision

With the exception of the gap dimension, the size tolerances and spacing tolerances of evaporated patterns can be computed simply (assuming high vacuum conditions) from the area the source presents to the substrate, and the ratio of mask-to-substrate to source-to-substrate distance. The mechanical jig described earlier uses a wire and a separate mask to define the electrode pattern. Since the substrate must move with respect to the wire, and since the mask must be moveable with respect to the wire, a minimum mask to substrate distance equal to the wire diameter plus suitable mechanical clearance is defined. The source-to-substrate distance is dictatated by the size of the evaporation chamber. Thus a size and position tolerence which is independent of the mask pattern can be computed in fractions of an inch. As the device size and spacing is reduced, this tolerance becomes a greater and greater percentage of the device dimension.

The fact that the wire which produces the source-drain separation must be spaced away from the substrate creates an additional limitation. For a given wire to substrate spacing, a certain size penumbra extending from adjacent edges of the source and drain can be expected. The source-drain separations can be no less than twice the penumbra width, or a short circuit of the gap will take place.

4. Lifetime

At present the electronic properties of a TFT are not constant with time, whether the device is in use or in storage. There is a general decay in the useful properties which sometimes can be related to atmospheric conditions and sometimes cannot. Frequently, the decay can be prevented or prolonged, and

sometimes the effect can be reversed and the device properties improved. These problems are being studied by other groups at RCA Laboratories, but their solution is a requisite to making satisfactory integrated circuits.

D. Approaches Taken

1. Uniformity

The pinholes in the insulator produce shorts from the gate to the semiconductor or from the gate to the source or drain electrode. Thus the presence of a pinhole results in device failure. Thicker insulating layers have fewer pinholes but reduce the controlling effect of the gate electrode. A certain random pinhole density can be expected in any thin evaporated layer, and this density is increased if the surface roughness is of the order of magnitude of the layer thickness. Silicon monoxide was used as the insulator in the majority of the fabrication attempts, and sufficient variation in its properties has been observed to justify an alternate choice for an insulating material. Three approaches were taken:

a. Cold Deposition of Silicon Dioxide

An attempt was made to deposit silicon dioxide on a substrate by reacting silicon tetrachloride with water vapor in a low-humidity chamber. The films thus produced were highly porous and this approach was abandoned.

b. High Temperature Deposition of Silicon Dioxide

Silicon dioxide films were formed on quartz substrates (and over evaporated gold electrodes) by the chemical cracking of silane (tetraethyl orthosilicate). The films thus produced had few pinholes and excellent breakdown strength, but lacked thickness uniformity. It is not certain whether the variation in thickness was sufficient to cause uniformity problems. The reaction takes place in a furnace at 700°C, and since CdS is not stable at these tempera-

tures, this process requires a reversed sequence of fabrication steps. That is, the gate is deposited first, the silicon dioxide second, the cadmium sulfide layer third, and the source-drain electrodes last.

c. Electrolytic Anodization of Aluminum

An investigation of aluminum oxide films formed by anodization of aluminum in a three percent solution of ammonium citrate yielded very promising results. The oxide films were extremely uniform, had few pinholes, good insulation properties, and were easily reproducible. Since CdS is slightly soluble in water, this process also requires the reverse sequence of fabrication steps described above, except that the insulating layer is formed by anodizing. This technique is also very promising as a method one might use in capacitor dielectric fabrication.

The reverse sequence of fabrication steps has one additional advantage. Since it is easier to produce a smooth insulator surface than to produce a smooth CdS surface, this procedure yields a smoother CdS-insulator interface, thus reducing the pinhole probability.

The variation in the CdS properties due to a nonuniform substrate temperature has been reduced somewhat by using a substrate heater which heats not only the substrate but the entire CdS evaporation jig (described below) and by allowing sufficient time for the assembly to come to thermal equilibrium. The heater consisted of a four inch infrared bulb suspended a few inches above the substrate and controlled by a variac.

2. Reproducibility

As was mentioned earlier, the best way to obtain reproducible results is to carefully control all the fabrication steps. The chief variant in the fabricated device, however, is the cadmium sulfide layer. The thickness,

departure from stoichimetric ratio, and surface condition of the CdS film greatly influence its electronic properties. These properties are in turn influenced by slight variations in substrate temperature, evaporant temperature, and surface cleanliness. To eliminate these difficulties advantage was taken of a cadmium sulfide evaporator design developed by L. Pensak a few years ago and nicknamed the "vacuum cow" (see Figs. 18a and 18b). Briefly, the "vacuum cow" is a separate evaporation chamber which is placed within a vacuum system and which can be opened during pumpdown but closed during evaporation. The chamber is basically a quartz vessel with a tube-like extension which holds the evaporant and a quartz wool sieve. The tube is surrounded by a shielded spiral heater which also serves to heat the wall of the quartz chamber. The top of the chamber contains the substrate heater, substrate shield and mask. After evacuating the chamber, the chamber is closed, and with the substrate shield in place, the cadmium sulfide evaporation begins. The initial moments of evaporation serve to "getter" the system providing a supercleaning of impurities within the chamber. The shield is then removed and deposition takes place upon the substrate. Since the chamber is closed, a higher vapor pressure of CdS obtains, and this permits higher substrate temperatures to be used. The higher substrate temperature produces CdS films which are closer in composition to the stoichimetric ratio. Since the shield is in place until deposition is already underway, negligible temperature variations on the substrate surface due to heating by the evaporant heater occur.

In spite of the evaporator design improvement some variation in CdS film resistivity is observed. It was found that a post-fabrication bake of the TFT in hydrogen or air raised the resistivity of the CdS layer. It is thus possible to treat the completed device in such a way as to modify its properties and make them more suitable.

Should it be found that the limited life of the TFT is due to an inherent surface property of CdS, it would be desirable to have an alternate choice for the semiconductor. Efforts had just begun at the close of the contract period to investigate evaporated silicon films. Initial results were encouraging, but an evaluation has not yet been attempted.

3. Device Dimensions and Precision

Under separate sponsorship, a device called the insulated gate field-effect transistor (see description elsewhere in this report) has been successfully used in integrated circuit fabrication. The device is similar in structure and performance to a TFT and masks used in the fabrication of this device were borrowed to determine if a more precise and reliable method of fabricating TFT's in large numbers on a single substrate is possible. The masks used for this purpose are shown in Figs. 19a, 19b, 19c. The mask in Fig. 19a is a "glass mask" which is used to expose a photoresist. The gap between source and drain is .0003" - .0004". The overall electrode size is .005" by .015". Very clean, sharp-edged source-drain patterns were produced on glass substrates using this technique. Since the mask is placed in contact with the substrate, tolerance problems are insignificant, and no penumbra is present. Fig. 19b is the mask used in the CdS deposition, and (rotated 90°) in the insulator deposition. Fig. 19c is the mask which produces the gate pattern. The width of the gate electrode is .0006". This narrow gate produces a minimum of geometrical capacitance. The masks in Figs. 19b and 19c are evaporation masks which are produced photographically and reinforced by electroplating. The device density achieved using such masks is 2200 TFT's per square inch. It was found that electrode, insulator, and semiconductor layers could be quite satisfactorily produced using these masks. All of the masks are placed in contact with the substrate in a jig

capable of precise alignment, so four individual evaporations are required.

An alternate method of fabricating the narrow gaps required has been developed. This new technique eliminates the need for high precision in the masks. A single electrode is deposited through a simple mask formed by photoetching techniques. The second electrode is then deposited through a similar mask, but the evaporation is done at an angle. If a sharp edge has been created on the first electrode, its shadow will define a gap between the two electrodes. The thickness of the first evaporation, the steepness of the sharp edge, and the angle of evaporation determine the gap width. Gaps of one micron (.00004 inch) have been obtained in this way (Fig. 20). The semiconductor and insulator are put in the gap and then a broad control electrode placed over the gap. By angle evaporation of the insulator it can be made much thicker over the source-drain electrodes than in the gap so the parasitic capacity from gate to the source and drain is minimized. With such narrow gaps it is possible to greatly improve the frequency characteristics of the device. Other semiconductors can also be tried which may improve the life characteristics over those experienced with CdS.

IV. ALTERNATE FORMS OF INSULATED GATE TRANSISTORS

Concurrent to the work on the TFT, a new type of insulated-gate field-effect transistor has been developed. In order to distinguish this device from other types of insulated-gate transistors it has been called the MOS transistor. This name is derived from the metal-oxide-semiconductor contact used. The operation of this transistor is similar to that of the TFT. The major difference between the two devices is the method of fabrication. The MOS transistors are produced on a silicon substrate by diffusing heavily doped source and drain contacts into the silicon and then thermally growing a silicon dioxide layer between them. A metal gate is then put on top of the silicon dioxide insulator. As with the TFT, the flow of majority carriers (electrons) from source to drain is controlled with a positive gate bias.

These transistors are presently being made with great success. Arrays of 2000 transistors on a one inch substrate have been fabricated with yields that have exceeded 90%. Presently, several different integrated circuits are being fabricated.

The MOS transistor has not suffered from the problem of its electrical characteristic deteriorating with time. Fig. 21 shows the volt-ampere characteristic of a typical MOS transistor. The input capacitance of these transistors is of the order of 1 pf. As a result of this low input capacitance the switching speed of the transistor is in the nanosecond range. A more detailed discussion of the MOS transistor is presented in The Air Force Scientific Report No. 1 entitled Insulated Gate Field Effect Silicon Triodes, Contract No. AF19(604)-8836.

V. CONCLUSIONS

During the period of this contract, significant advances were made in the application of the TFT to digital applications. Individual TFT's were operated in switching circuits at rates of 1 megacycle under realistic load conditions. The internal switching speed of the TFT was found to be on the order of several nanoseconds. This verifies that the TFT can operate at much higher rates if the parasitic capacities are reduced. A technology to produce very narrow gaps, which would increase the gain bandwidth of the device by an order of magnitude, has been developed. Variations in evaporated cadmium sulfide film properties have been reduced, and it is now possible to batch fabricate TFT's, with good batch to batch reproducibility. Furthermore, a reliable way of fabricating insulating layers has been found which increases the yield of good units within a batch. Finally, the feasibility of producing large numbers of fine dimensioned, closely spaced TFT's on a single insulating substrate has been demonstrated. The crucial problem is to find the mechanism which causes the decay of the characteristics with time. Once this problem has been solved, the economical vacuum fabrication of active integrated circuits is not far off.

The present availability of an alternate form of insulated gate majority carrier device allows circuit work to continue toward the evaluation of the forms of registers which can ultimately be built in integrated form.

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8. R. Bockemuehl, Proceedings of the IRE, 48, 875 (1960)
9. P. K. Weimer, RCA Review, 12, (1951)
10. P. K. Weimer, et al, IRE Transactions on EL Devices, 147 (July 1960)
11. P. K. Weimer, "Evaporated Thin Film Triodes," paper presented at the Solid State Devices Research Conference, Stamford, June 1961
12. P. K. Weimer, Proceedings of the IRE, 50, 1462 (1962)

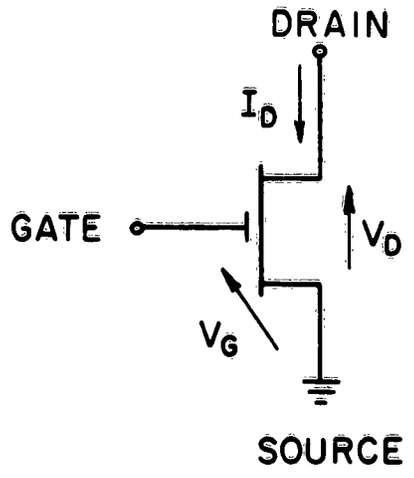
VII. LIST OF FIGURES

18. (a) "Vacuum Cow" evaporator. Heater has been lowered from its operating position, exposing the tube-like extension of the quartz chamber. Substrate holder and shield are in the extended position used during the pumpdown cycle; (b) top view of "Vacuum Cow" as it appears during CdS deposition.

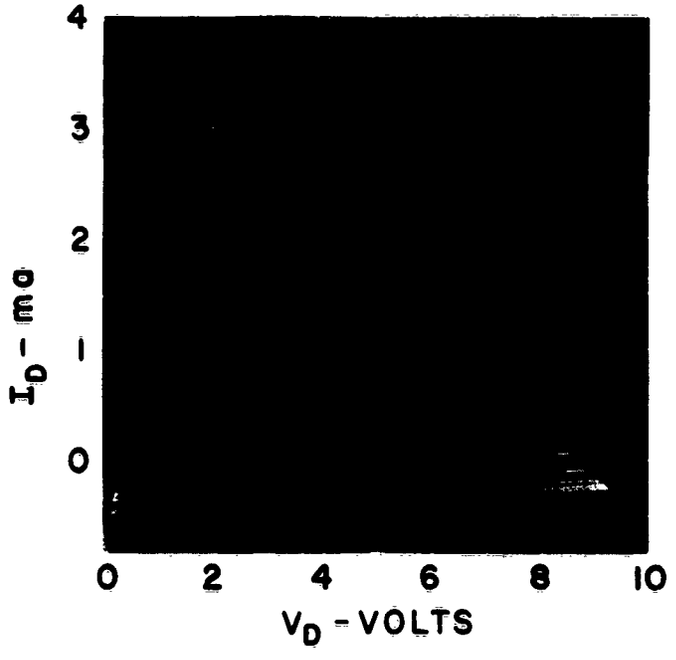
19. Sections of photographically produced high device density masks - (a) glass mask used to expose photoresist for source-drain pattern; (b) evaporation mask used for CdS and (when rotated 90 degrees) insulating layers; (c) evaporation mask used to produce gate pattern

20. A one micron (0.00004 inch) gap made by shadow evaporation

21. Volt-ampere characteristic of an MOS transistor



(a)



V_G: 0 TO +6 VOLTS IN 0.5 VOLT STEPS

(b)

FIG. 1 (a) TFT SYMBOL, (b) TYPICAL TFT VOLT-AMPERE CHARACTERISTICS

TIME - 50 NANOSECONDS/DIV

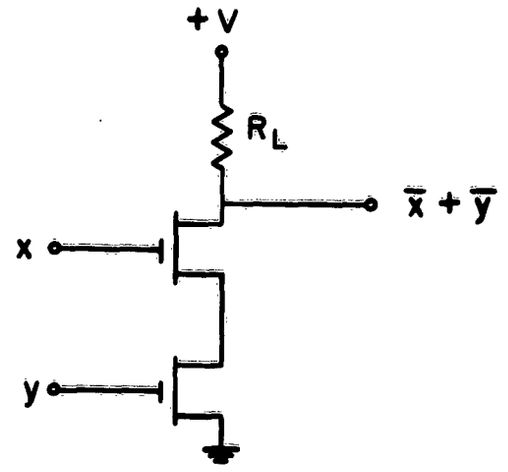
V_{DD} = + 8 VOLTS

V_G - + 8 VOLT PULSE

R_D = 10,000 OHMS

SOURCE IMPEDANCE: 50,500,2K-OHMS

FIG. 2 PULSED TFT OUTPUT RISE TIME FOR VARIOUS SOURCE IMPEDANCES



(a)

OUTPUT

BOTH INPUTS ON

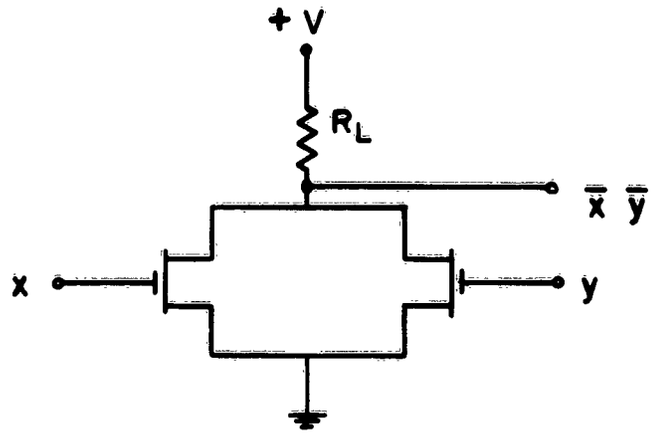
y INPUT ONLY

x INPUT ONLY

BOTH INPUTS OFF

(b)

FIG. 3 (a) TFT NAND GATE, (b) NAND GATE WAVEFORMS; R_L = 3 K OHMS, V = 8 VOLTS, SCALES: VERTICAL - 2 VOLTS/DIVISION, HORIZONTAL - 2 μ SEC/DIVISION



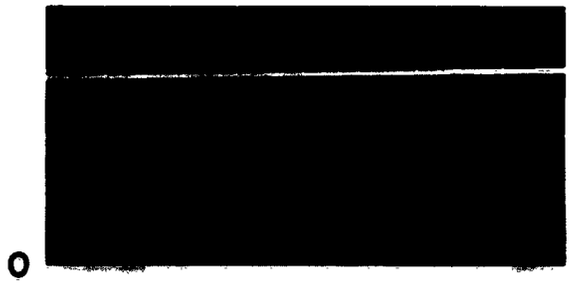
INPUTS

OUTPUTS

BOTH INPUTS ON

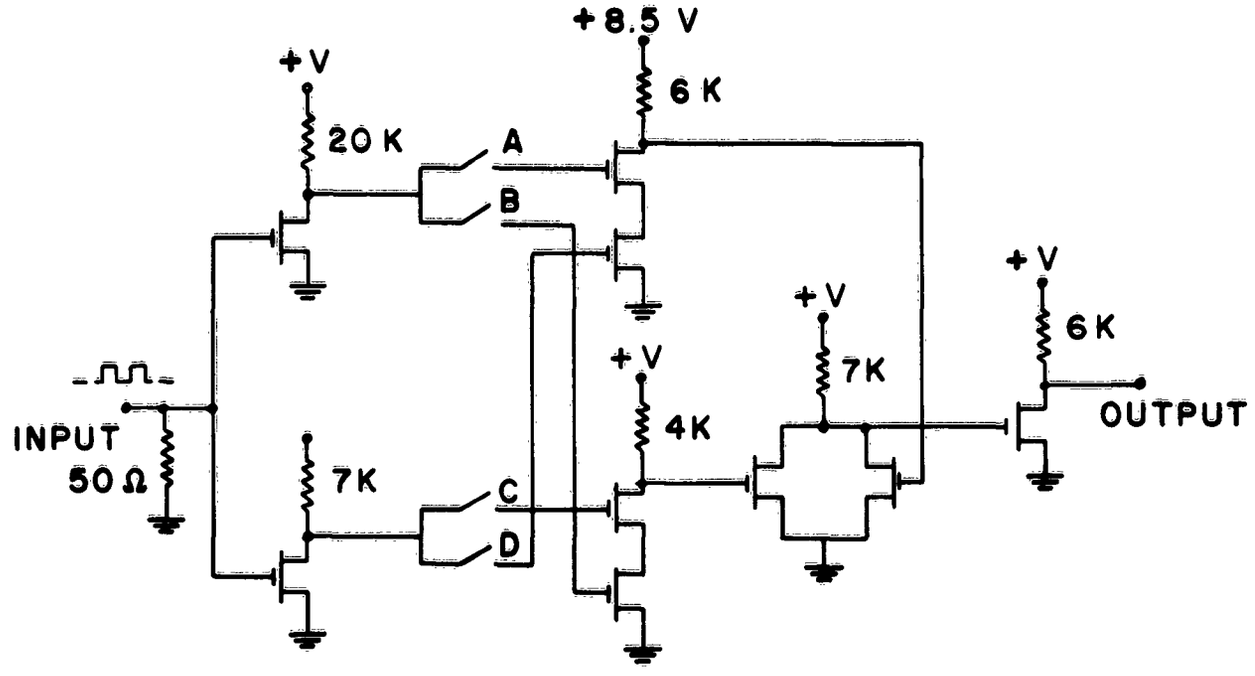
LEFT INPUT ON

RIGHT INPUT ON



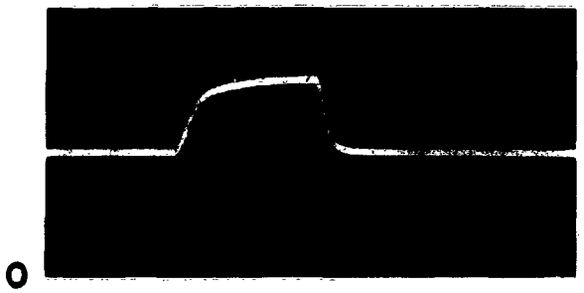
BOTH INPUTS OFF

FIG. 4 (a) TFT NOR GATE (b) NOR GATE WAVEFORMS
R_L = 1.5 K OHMS, V = 8 VOLTS
SCALES: VERTICAL - 2 VOLTS / DIVISION
HORIZONTAL - 2 μ SEC / DIVISION

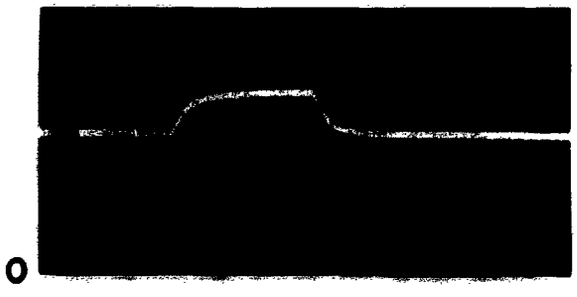


(a)

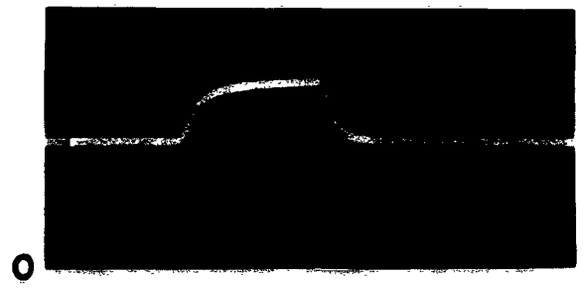
INPUT



OUTPUT-ALL SWITCHES ON



OUTPUT SWITCH A OFF



OUTPUT SWITCH C OFF

FIG. 5 (a) COMBINATIONAL LOGIC CIRCUIT
(b) CIRCUIT WAVEFORMS
SCALES: VERTICAL - 2 VOLTS/DIVISION
HORIZONTAL - 5 μ SEC/DIVISION

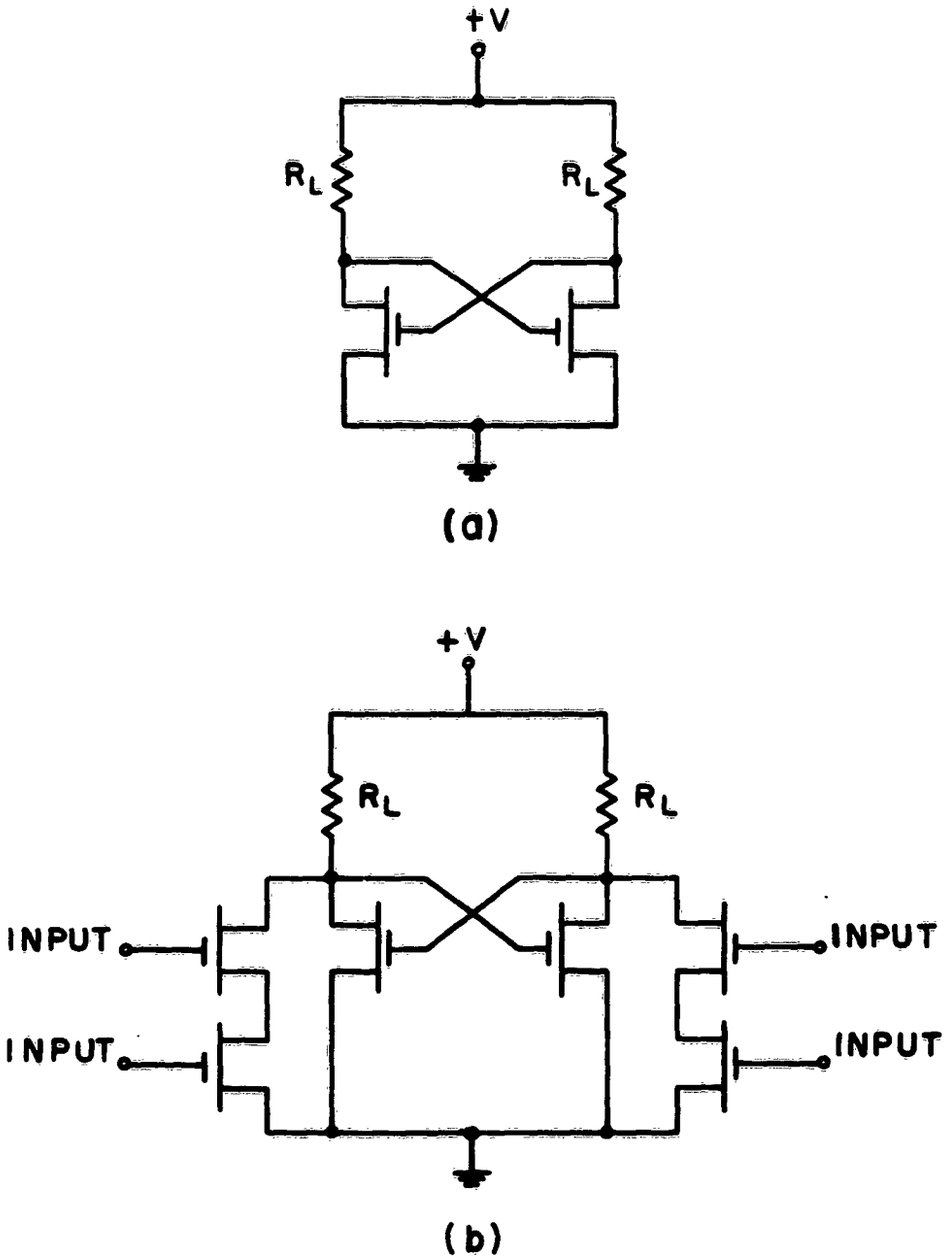
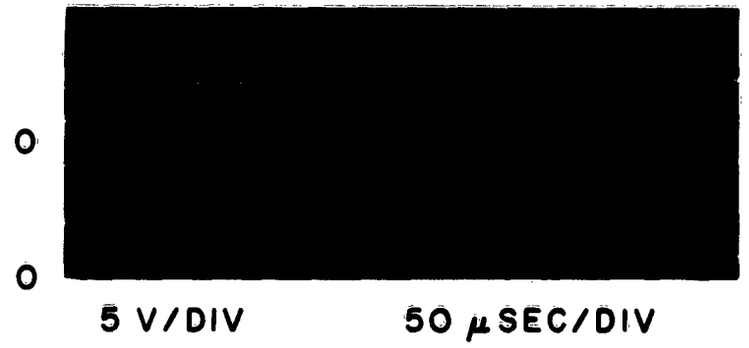
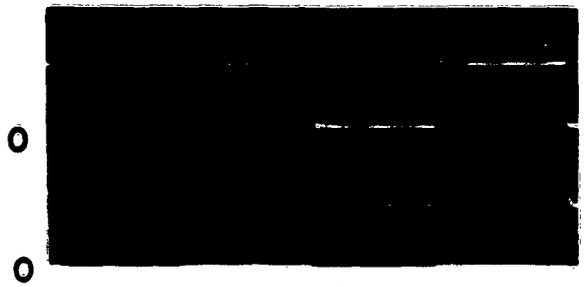


FIG. 6 (a) BASIC TFT FLIP-FLOP (b) TFT FLIP-FLOP WITH PROVISIONS FOR SET-RESET TRIGGERING



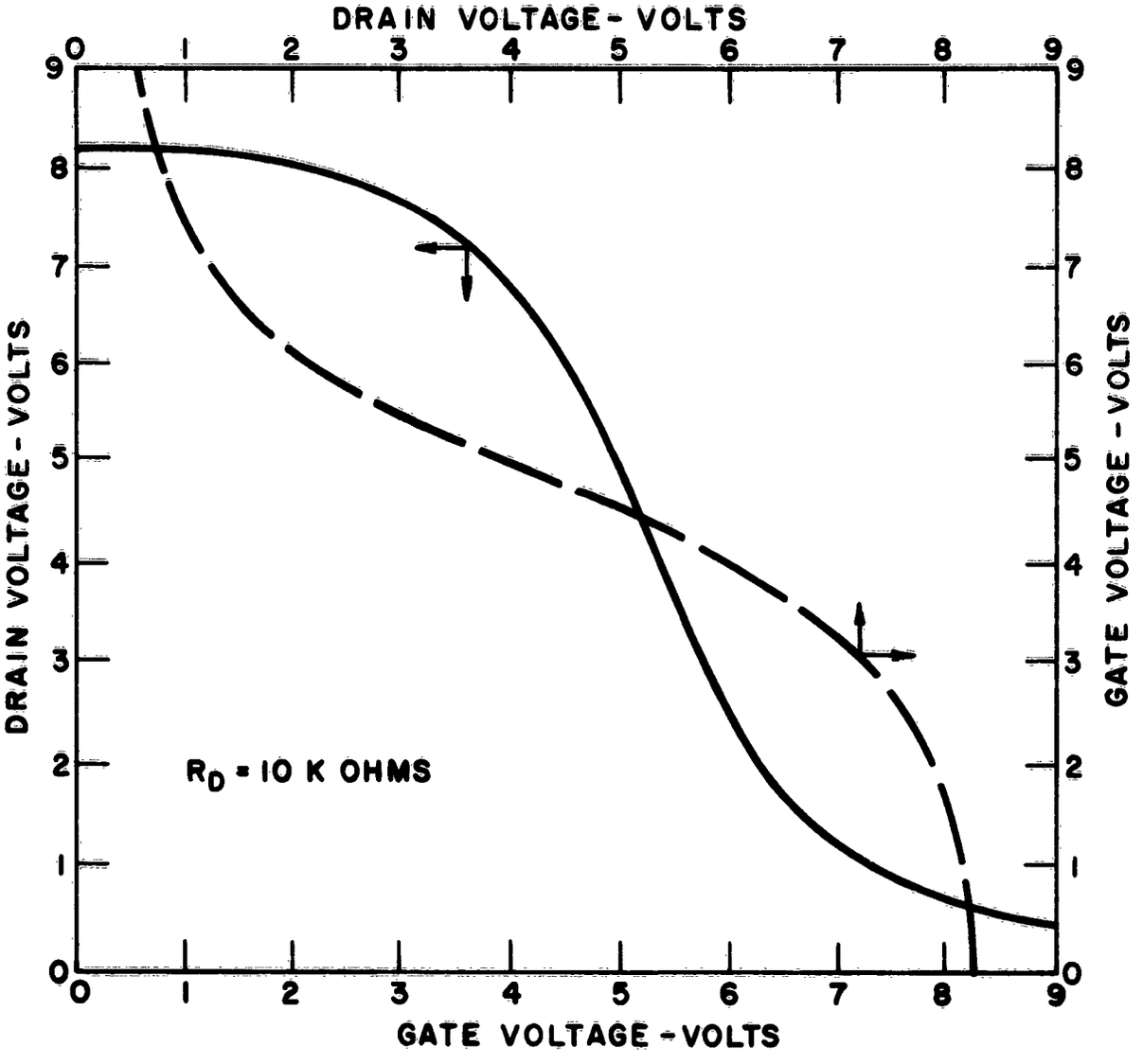
(a)



(b)

(C)

FIG. 7 WAVEFORMS OF TFT FLIP-FLOPS (a) TRIGGER FLIP-FLOP, TRIGGERED FROM A TFT AMPLIFIER THROUGH STEERING DIODES (b) SET-RESET FLIP-FLOP TRIGGERED FROM LOW IMPEDANCE PULSE GENERATORS (c) SET-RESET FLIP-FLOP TRIGGERED THROUGH TFT'S



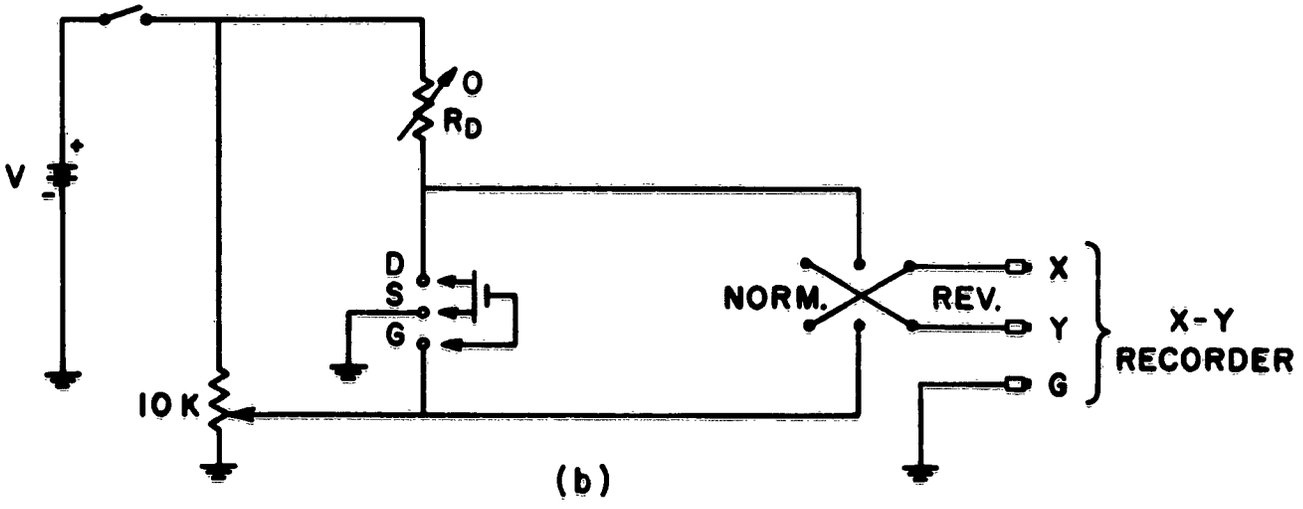


FIG. 8 (a) TFT FLIP-FLOP CHARACTERISTIC, (b) CIRCUIT FOR OBTAINING FLIP-FLOP CHARACTERISTIC

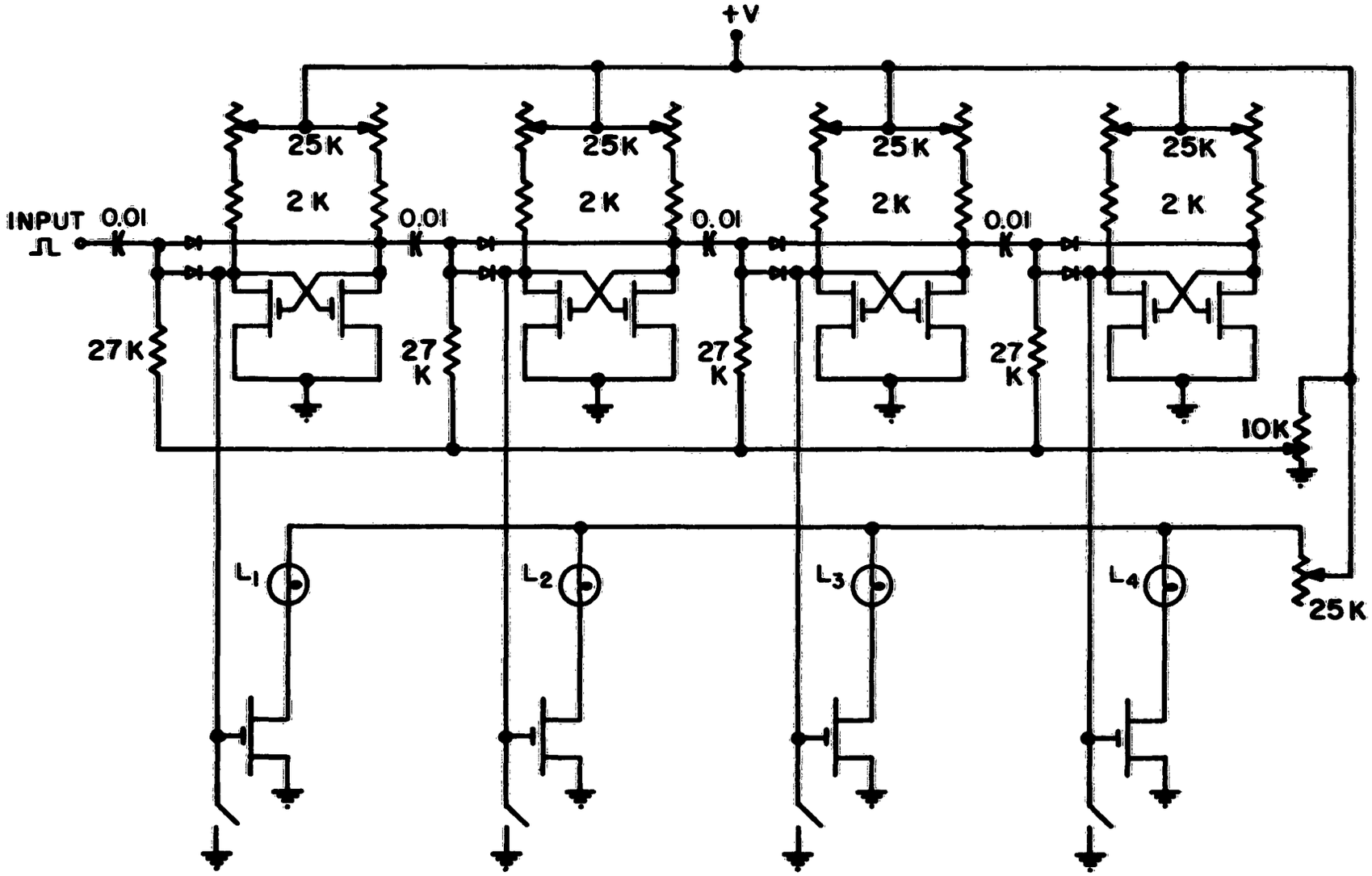


FIG. 9. SCALE OF 16 COUNTER

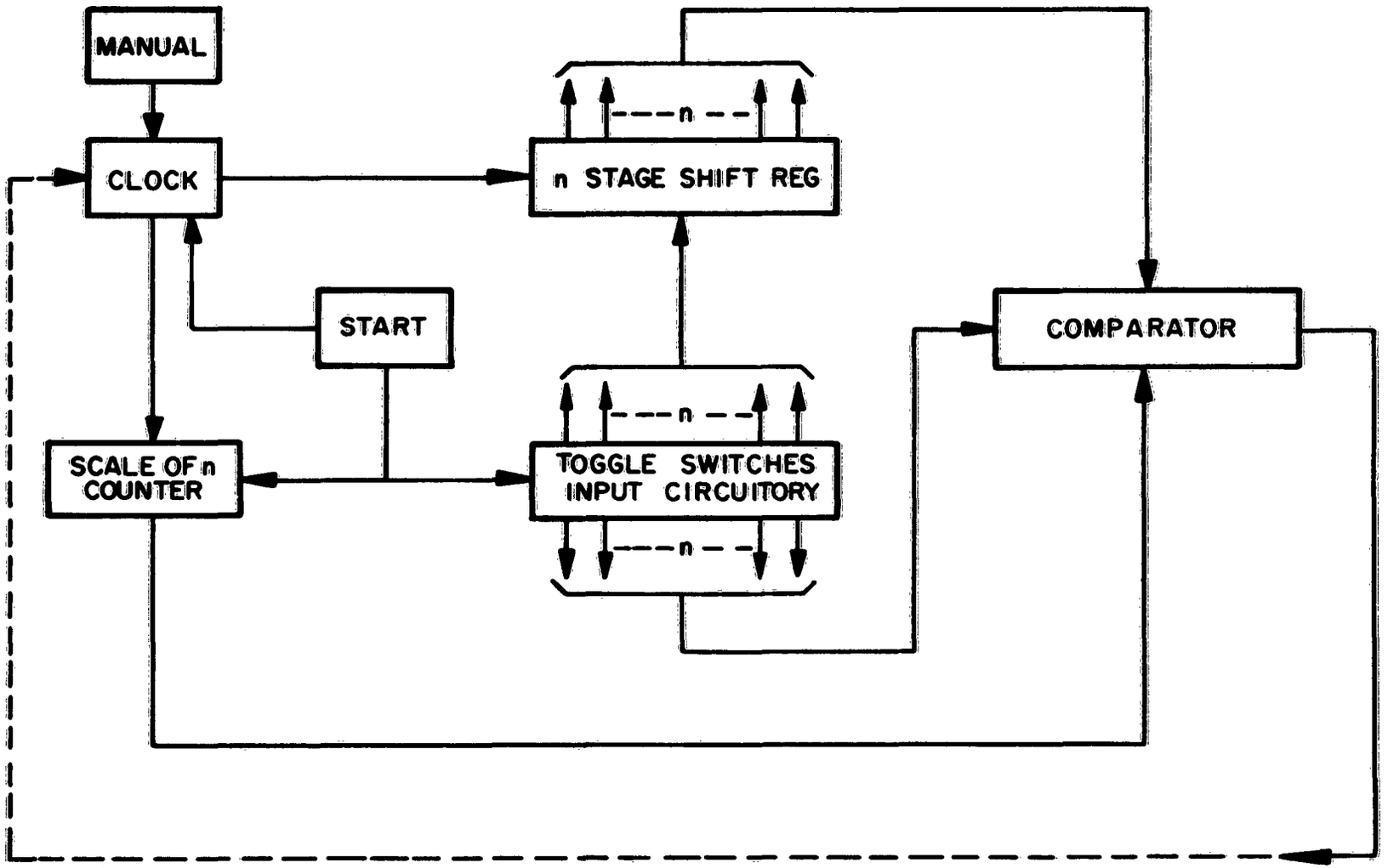


FIG. 10 SHIFT REGISTER AND COMPARATOR BLOCK DIAGRAM

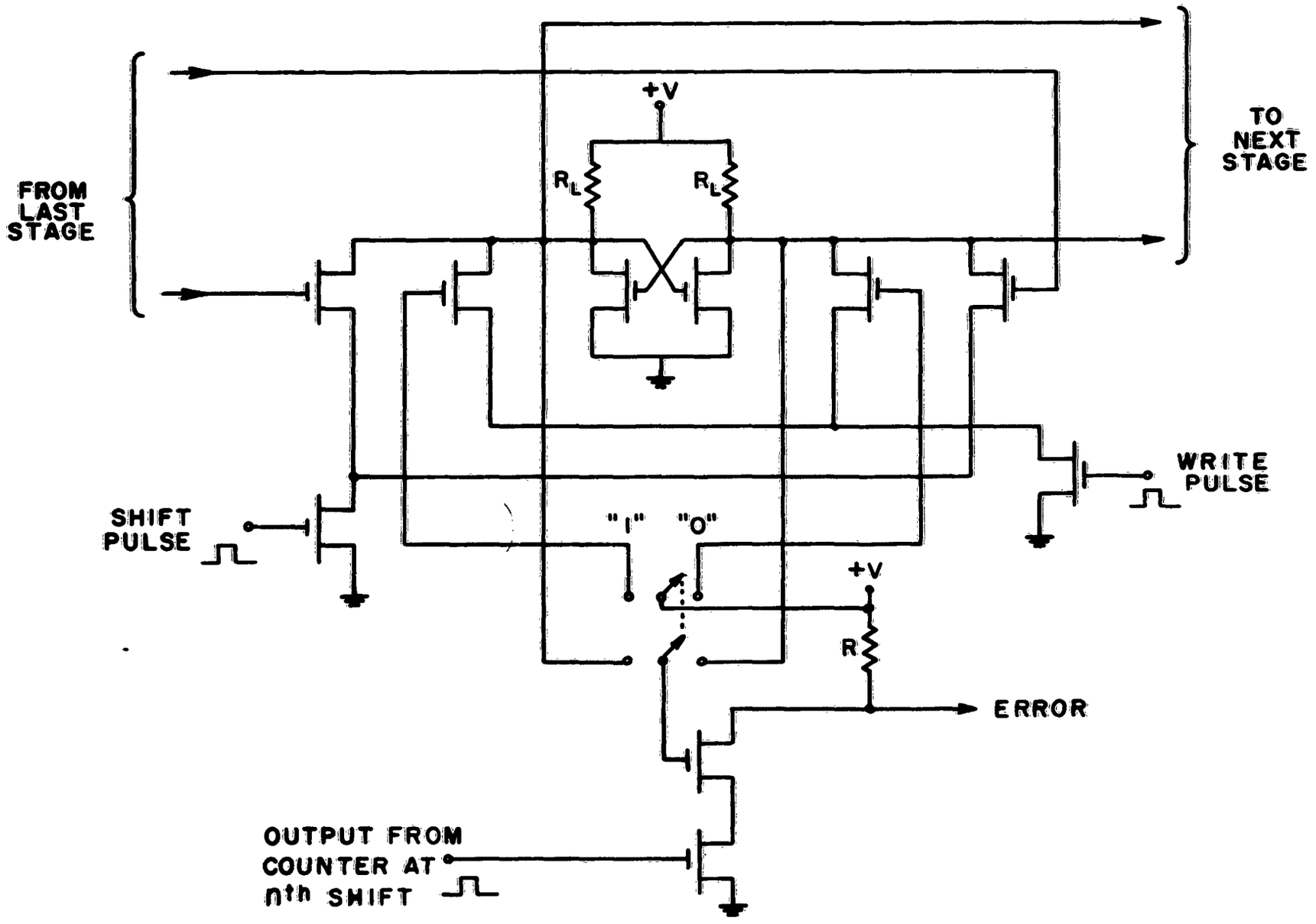


FIG. 11 ONE STAGE OF SHIFT REGISTER

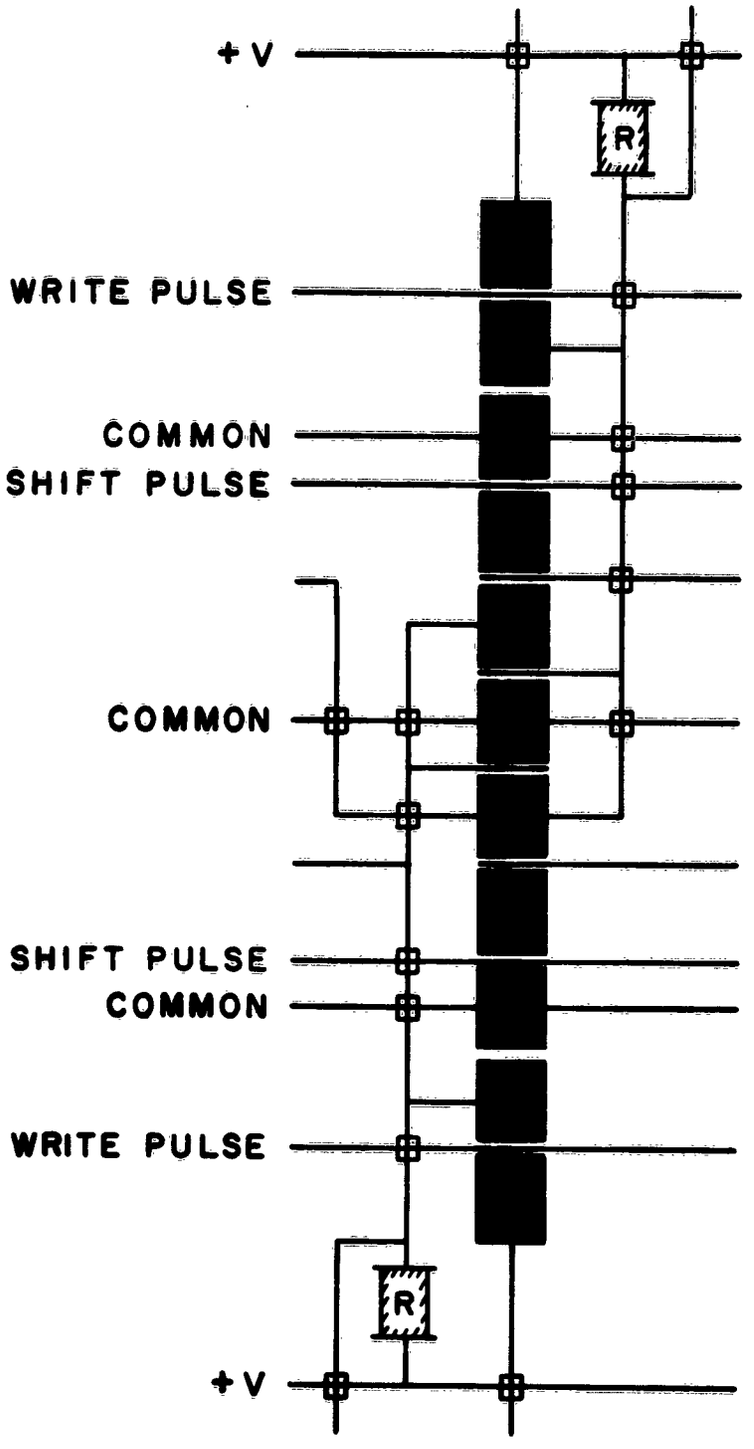


FIG. 12 MOCK-UP OF ONE STAGE OF SHIFT REGISTER THE STAGE IS COMPLETELY FABRICATED BY VACUUM DEPOSITION

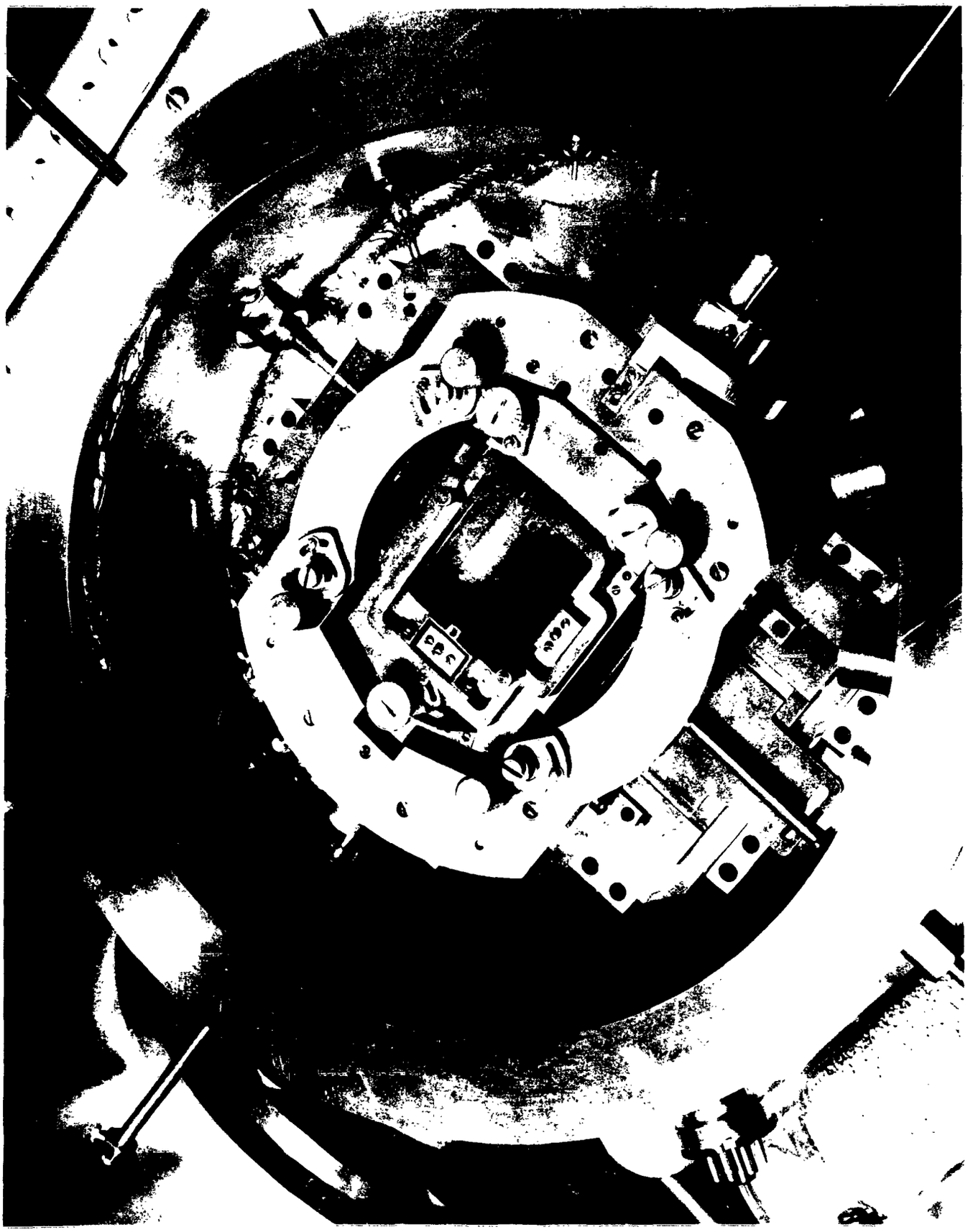
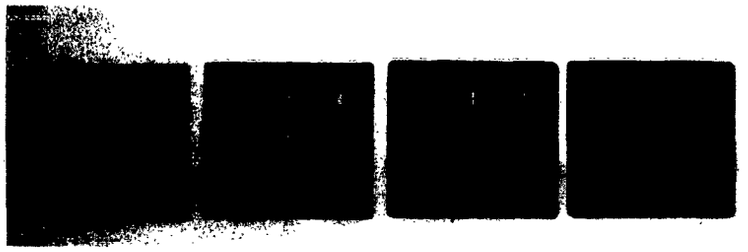


FIG. 13 PRECISION JIG USED IN DEPOSITING ELECTRODES AND INSULATOR



a b c d

FIG. 14 SET OF MASKS USED IN FABRICATING A THREE BY THREE TFT ARRAY. (a) SOURCE & DRAIN MASK (b) CADIUM SULPHIDE MASK (c) INSULATOR MASK (d) GATE MASK

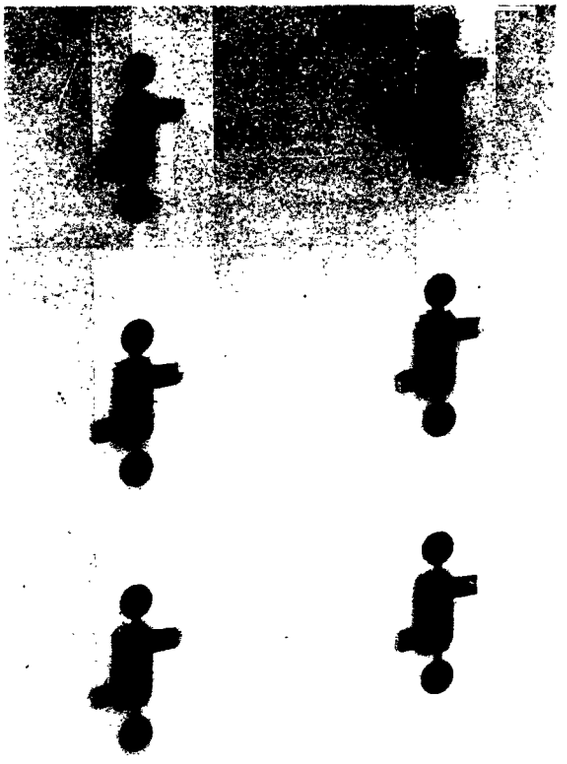


FIG. 15 SET OF SIX TFT'S FABRICATED WITH ABOVE MASKS

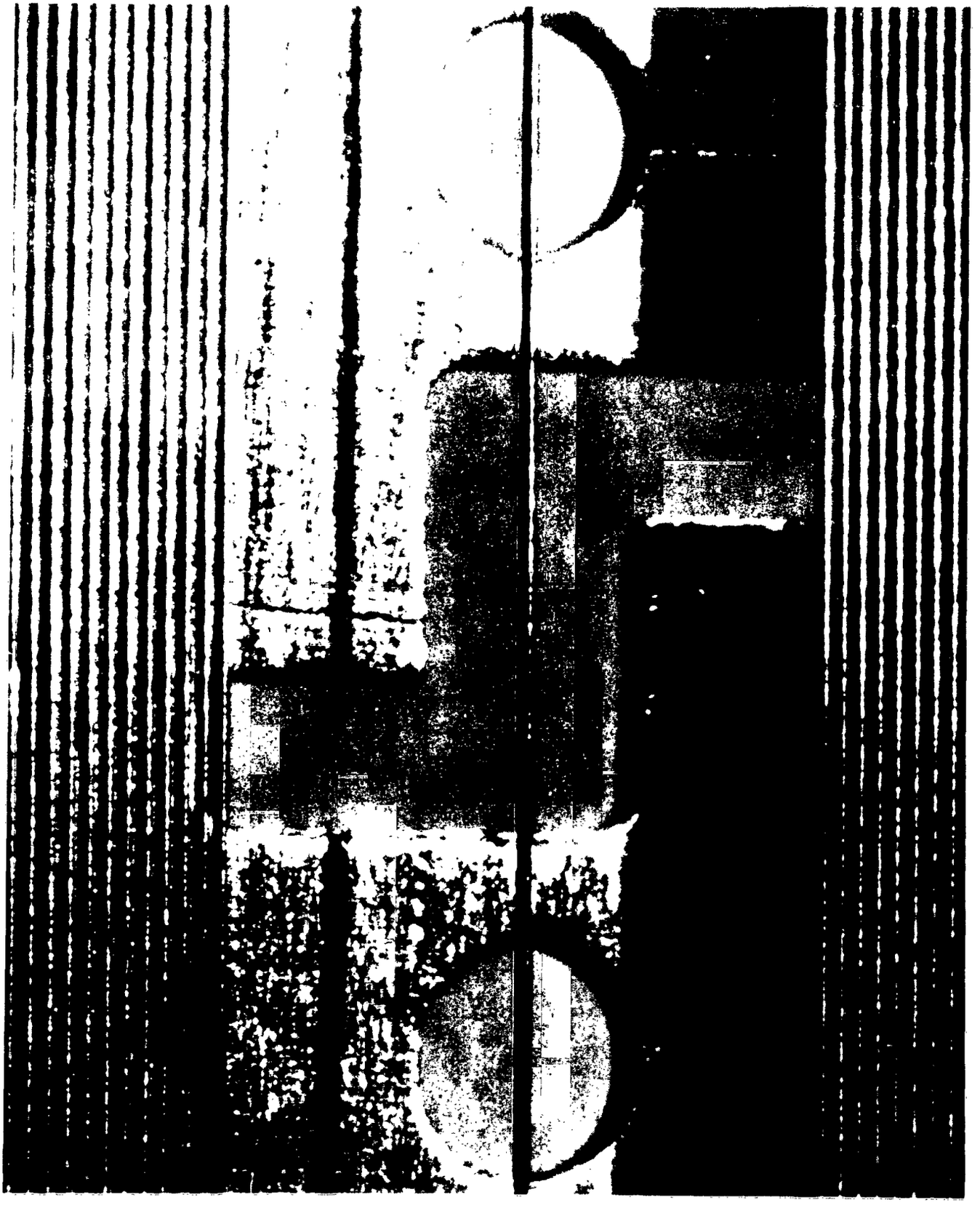


FIG. 16 VIEW FROM SUBSTRATE SURFACE LOOKING TOWARD EVAPORANT SOURCE THROUGH ONE OF THE PATTERNS IN THE SOURCE AND DRAIN MASK. NOTE THE WIRE USED TO PROVIDE THE GAP BETWEEN ELECTRODES

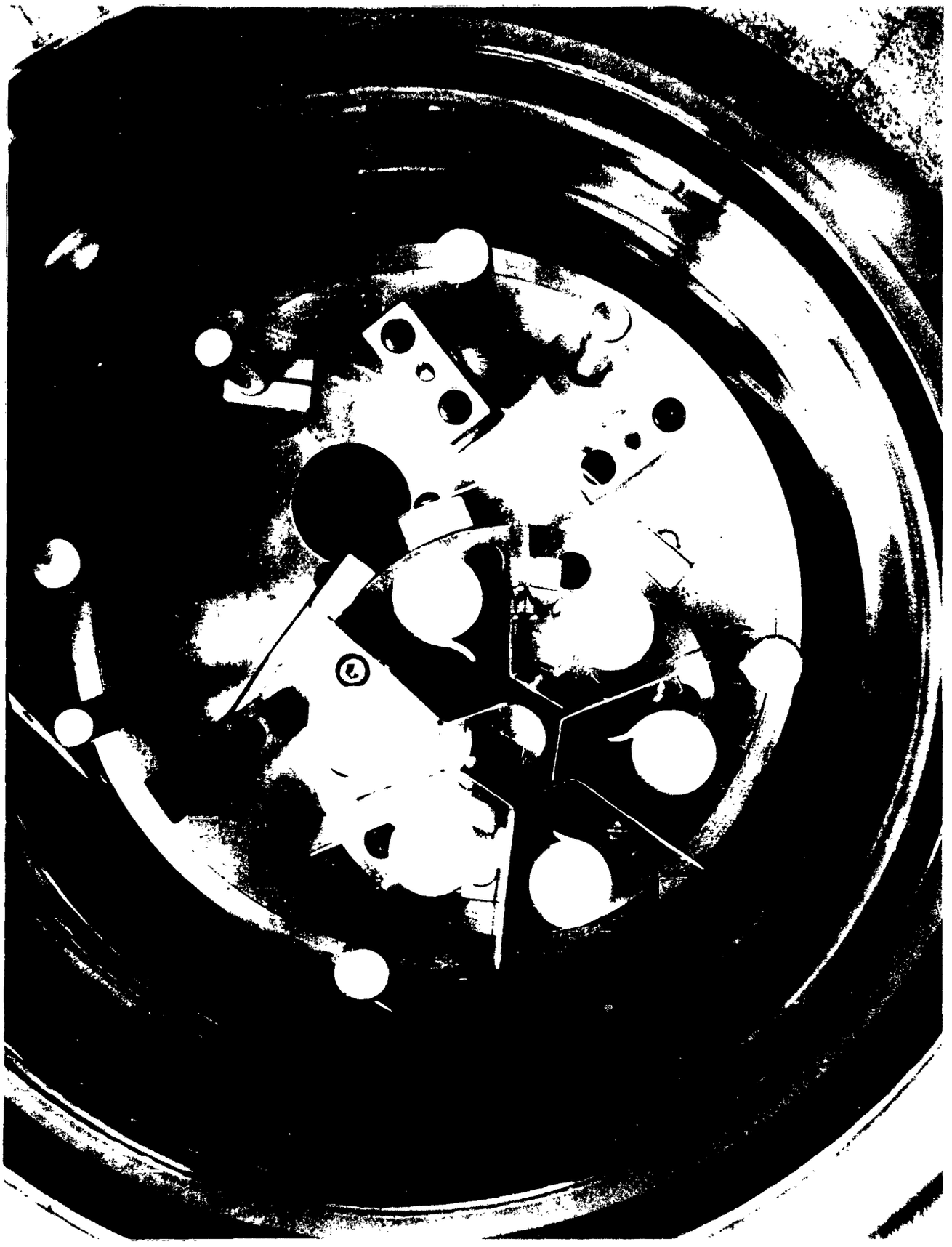


FIG. 17 TOP VIEW OF TURRET EVAPORATOR USED IN ELECTRODE AND INSULATOR DEPOSITIONS

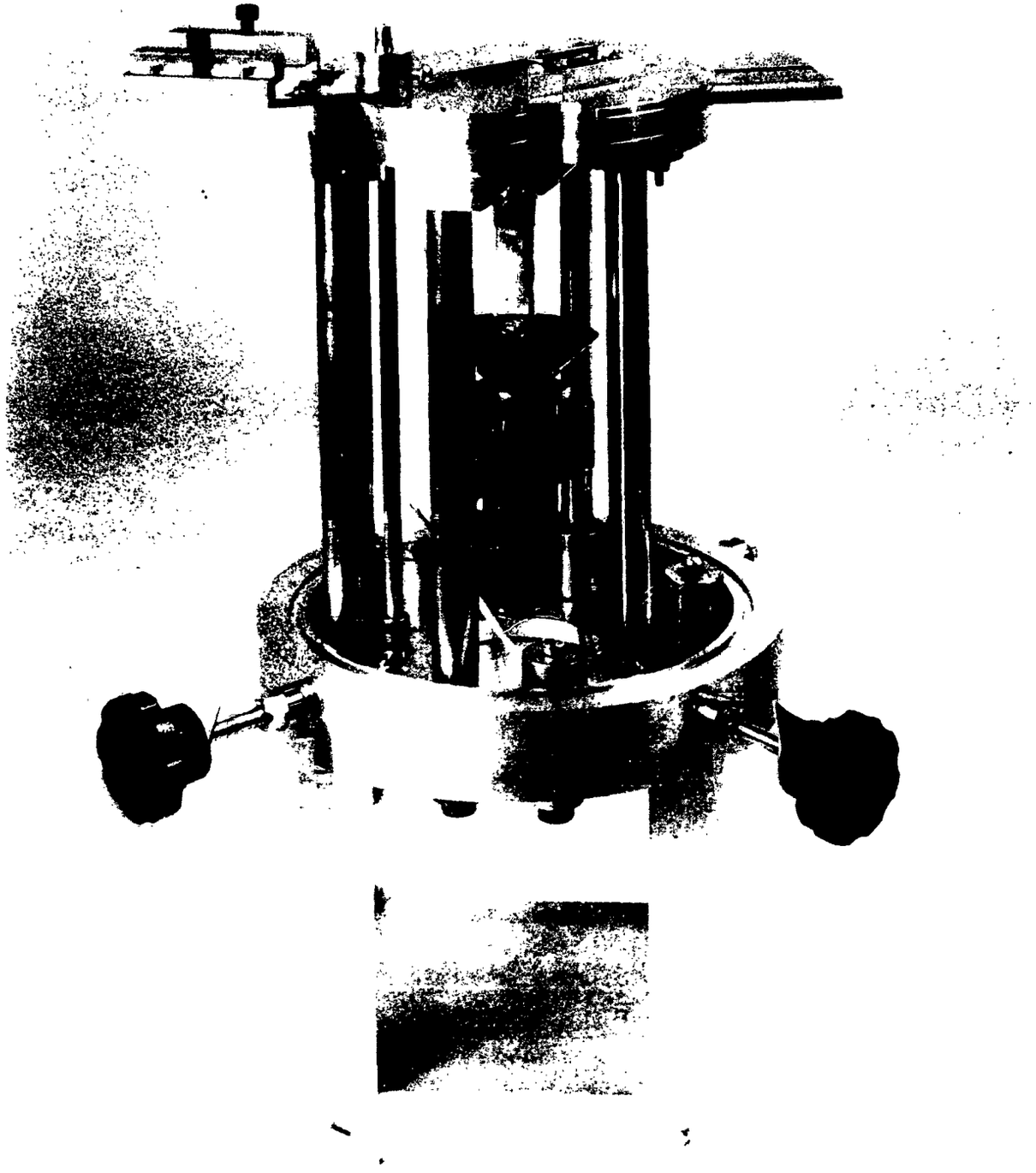


FIG. 18a "VACUUM COW" EVAPORATOR. HEATER HAS BEEN LOWERED FROM ITS OPERATING POSITION, EXPOSING THE TUBE-LIKE EXTENSION OF THE QUARTZ CHAMBER. SUBSTRATE HOLDER AND SHIELD ARE IN THE EXTENDED POSITION USED DURING THE PUMPDOWN CYCLE

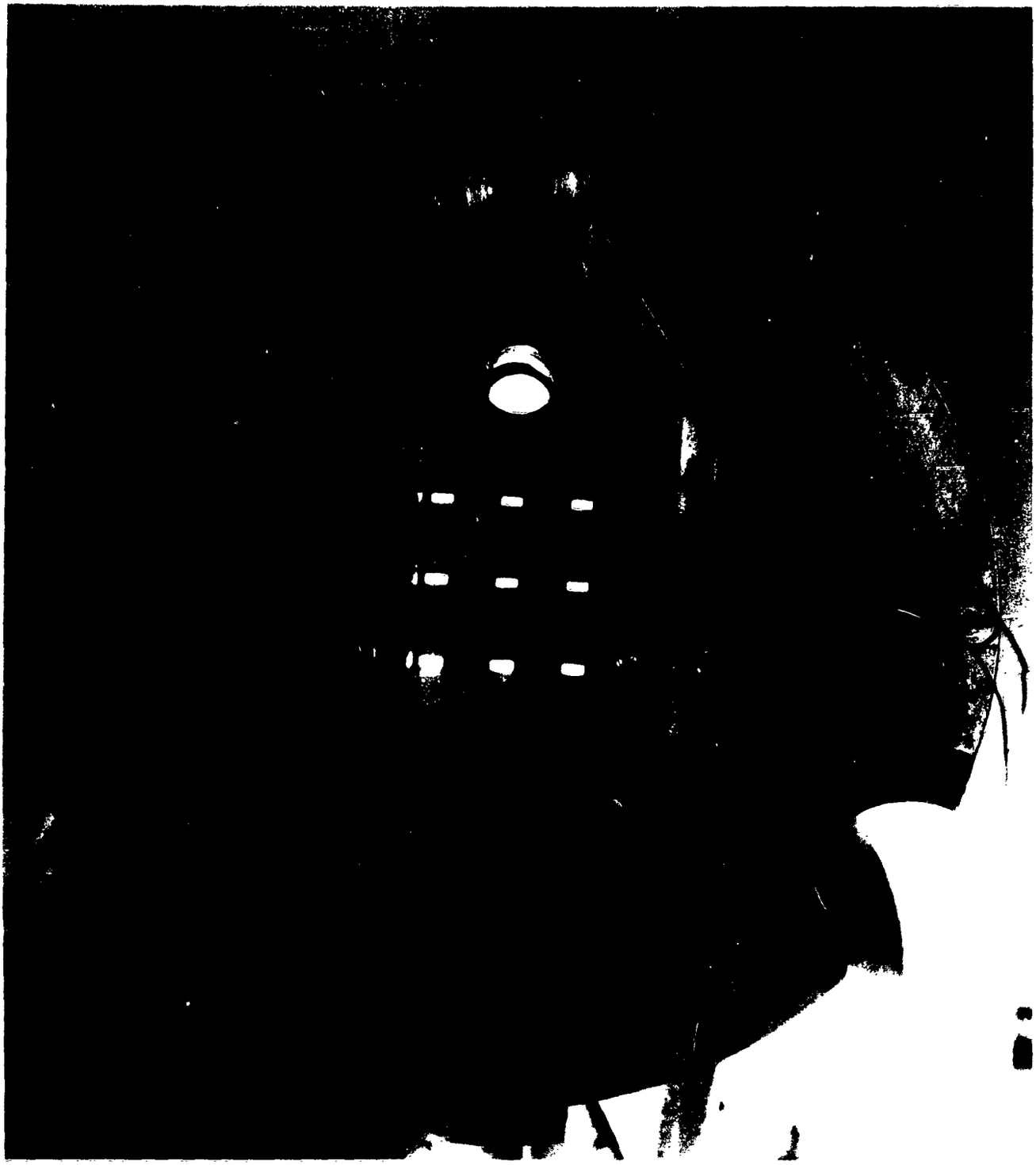


FIG. 18b TOP VIEW OF "VACUUM COW" AS IT APPEARS DURING CdS DEPOSITION

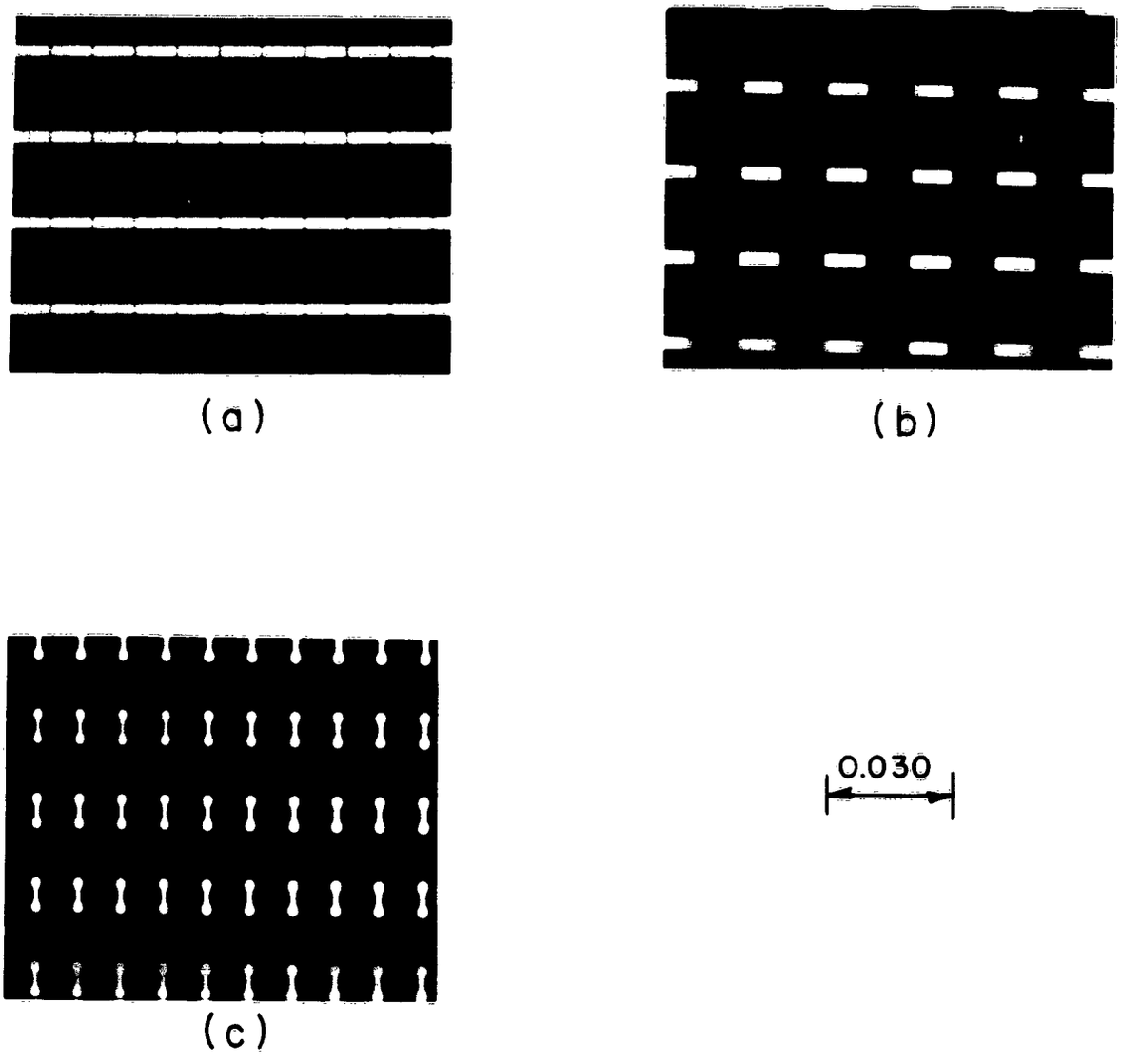


FIG. 19 SECTIONS OF PHOTOGRAPHICALLY PRODUCED HIGH-DEVICE-DENSITY MASKS

(a) GLASS MASK USED TO EXPOSE PHOTORESIST FOR SOURCE-DRAIN PATTERN

(b) EVAPORATION MASK USED FOR CdS AND (WHEN ROTATED 90 DEGREES) INSULATING LAYERS

(c) EVAPORATION MASK USED TO PRODUCE GATE PATTERN

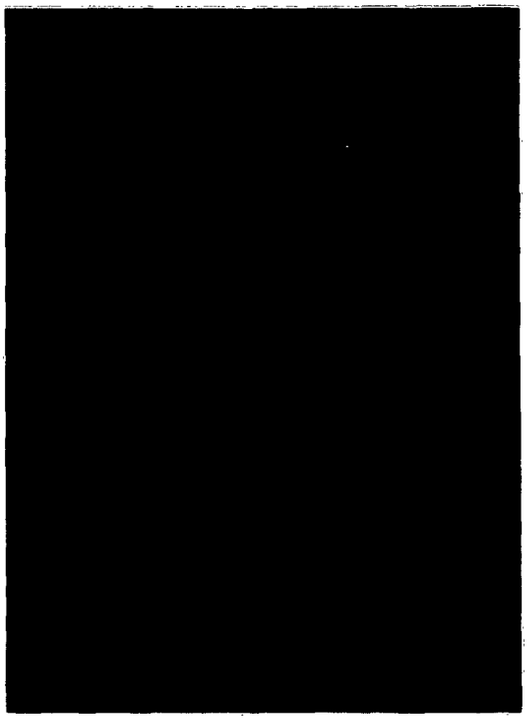


FIG. 20 A ONE - MICRON (0.00004 INCH) GAP MADE BY SHADOW EVAPORATION

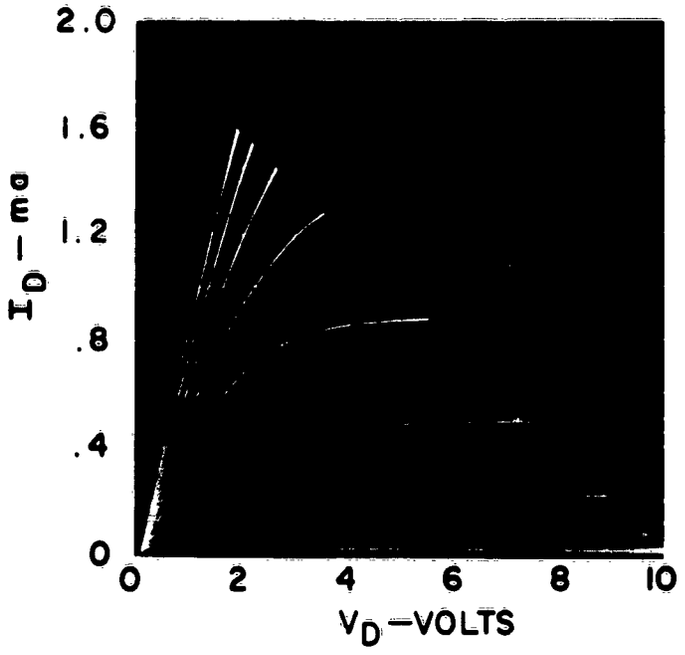


FIG. 21 VOLT—AMPERE CHARACTERISTICS OF AN MOS TRANSISTOR